Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A system for compensating for phase differences between ~~a plurality of~~ first and second clock signals ~~associated with a plurality of signal levels~~, the first clock signal driving a first circuit that is powered by a first supply voltage level, and the second clock signal driving a second circuit that is powered by a second supply voltage level different than the first supply voltage level, the circuit comprising:

at least one phase comparator ~~for comparing~~ adapted to receive the first and second clock signals, to compare a phase of ~~a~~ the first clock signal ~~associated with a first signal level~~ with a phase of ~~a~~ the second clock signal ~~associated with a second signal level,~~ and ~~for generating~~ to generate at least one compensation signal indicative of a phase difference between the first clock signal and the second clock signal;

at least one delay adjuster coupled to the at least one phase comparator and responsive to the at least one compensation signal, for delaying the first clock signal to compensate for the phase difference between the first clock signal and the second clock signal.

2. (original) The system of claim 1 wherein the at least one delay adjuster comprises at least one adjustable delay buffer.

3. (currently amended) The system of claim ~~2~~ 1 wherein the at least one phase comparator comprises:

a rising edge phase comparator for comparing a rising edge of the first clock signal with a rising edge of the second clock signal, for generating at least one rising edge compensation signal

indicative of a phase difference between the rising edge of the first clock signal and the rising edge of the second clock signal; and

a falling edge phase comparator for comparing a falling edge of the first clock signal with a falling edge of the second clock signal, for generating at least one falling edge compensation signal indicative of a phase difference between the falling edge of the first clock signal and the falling edge of the second clock signal.

4. (currently amended) The system of claim 1 wherein the at least one ~~adjustable~~ delay ~~buffer~~ adjuster:

delays the rising edge of the first clock signal in response to the rising edge compensation signal; and

delays the falling edge of the first clock signal in response to the falling edge compensation signal.

5. (currently amended) The system of claim 2 wherein the at least one adjustable delay buffer comprises:

at least one buffer transistor for buffering the first clock signal; and

at least one control transistor, responsive to the at least one compensation signal, for adjusting current flow through the at least one buffer transistor for controlling delay of the first clock signal through the at least one buffer transistor.

6. (currently amended) The system of claim 1 further comprising a plurality of buffers for generating the first clock signal and the second clock signal.

7. (original) The system of claim 6 wherein the plurality of buffers comprise a plurality of clock trees.

8. (currently amended) The system of claim 1 further comprising at least one power supply for providing ~~a plurality of~~ the first supply ~~voltages~~ voltage level and the second supply voltage level associated with the plurality of signal levels.

9. (currently amended) The system of claim 1 wherein the first clock signal and the second clock signal are derived from a common clock signal.

10-29. (cancelled)

30. (new) A method for compensating for phase differences between a plurality of clock signals associated with a plurality of signal levels, comprising the steps of:

modifying a signal level of a first clock signal associated with a first signal level to generate a second clock signal associated with a second signal level that is different than the first signal level;

comparing a phase of the first clock signal with a phase of the second clock signal to generate at least one compensation signal indicative of a phase difference between the first clock signal and the second clock signal; and

delaying the first clock signal to compensate for the phase difference between the first signal and the second signal.

31. (new) The method of claim 30 wherein:

the comparing step further comprises the steps of:

comparing a rising edge of the second clock signal to generate a rising edge compensation signal indicative of a phase difference between the rising edge of the first clock signal and the rising edge of the second clock signal; and

comparing a falling edge of the first clock signal with a falling edge of the second clock signal to generate a falling edge compensation signal indicative of a phase difference between the falling edge of the first clock signal and the falling edge of the second clock signal;

and the delaying step further comprises the steps of:

delaying the rising edge of the first clock signal in response to the rising edge compensation signal; and

delaying the falling edge of the first clock signal in response to the falling edge compensation signal.

32. (new) The method of claim 30 wherein the delaying step comprises selectively routing the first clock signal through at least one of a plurality of delay elements to compensate for the phase difference between the first clock signal and the second clock signal.